

CLAIMS

What is claimed is:

1 1. A memory system having a plurality of memories
2 each having a command decoder front end receiving incoming
3 command packets, and a set of at least one command
4 sequencer,

5 wherein said command decoder front end has
6 facilities for (1) at least partially decoding incoming
7 command packets, (2) issuing commands to at least one
8 sequencer in said set of command sequencers in response to
9 said incoming command packets, and (3) performing a first
10 group of at least one memory control step of a decoded
11 command in response to said incoming command packets,

12 and wherein each of said command sequencers has
13 facilities for performing a second group of memory control
14 steps of decoded commands issued to the command sequencer
15 from the command decoder front end.

1 2. A system according to claim 1, wherein said
2 command decoder front end further has facilities for
3 assembling each of said incoming command packets from a
4 respective plurality of consecutive incoming command words.

1 3. A system according to claim 1, wherein said
2 command decoder front end further has facilities for

3 determining whether or not to perform said first group of
4 memory control steps for a given incoming command packet.

1 4. A system according to claim 1, wherein each of
2 said incoming command packets has associated therewith a
3 respective desired latency value, and wherein said command
4 decoder front end further has facilities for performing
5 said first group of memory control steps for a given
6 incoming command packet only if the desired latency value
7 associated with said given command packet is below a
8 predetermined threshold latency value.

1 5. A system according to claim 4, wherein each of
2 said command sequencers further has facilities for
3 performing said first group of memory control steps for
4 said given incoming command packet, if said command decoder
5 front end does not perform said first group of memory
6 control steps for said given incoming command.

1 6. A system according to claim 4, wherein said
2 incoming command packets include a command type indicator,
3 and wherein said command decoder front end includes
4 facilities to determine the desired latency value for the
5 given command packet in dependence upon the command type
6 indicator in the given command packet.

1 7. A system according to claim 1, wherein the
2 facilities of said command decoder front end for issuing
3 commands to at least one sequencer in response to said
4 incoming command packets, issues such commands for a given
5 incoming command packet substantially simultaneously with
6 the performance by said command decoder front end of a
7 memory control step for said given incoming command packet.

1 8. A method for managing a memory system, for use
2 with an incoming command packet, comprising the steps of:

3 receiving said incoming command packet in a command
4 decoder front end;

5 said command decoder front end decoding said command
6 packet, issuing a command to a first command sequencer in
7 response to said command packet, and further performing a
8 first group of at least one memory control step in response
9 to said incoming command packet; and

10 said first command sequencer performing a second
11 group of at least one memory control step in response to
12 receipt of said command from said command decoder front
13 end.

1 9. A method according to claim 8, further
2 comprising the step of assembling said command packet from
3 a plurality of consecutive incoming command words.

1 10. A method according to claim 8, further
2 comprising the step of said first command sequencer
3 determining that said first group of memory control steps,
4 are performed by said command decoder front end,

5 further comprising the step of said first command
6 sequencer abstaining from performing said first group of
7 memory control steps in response to said step of
8 determining.

1 11. A method according to claim 8, wherein said
2 step of said command decoder front end issuing a command to
3 a first command sequencer in response to said incoming
4 command packet occurs substantially simultaneously with the
5 step of said command decoder front end performing a first
6 group of at least one memory control step in response to
7 said incoming command packet.

1 12. A method according to claim 8, further
2 comprising the steps of:

3 said command decoder front end further indicating a
4 latency value to said first command sequencer in

5 conjunction with said step of said command decoder issuing
6 a command to a first command sequencer; and

7 said first command sequencer inserting at least one
8 latency wait state in dependence upon said latency value
9 indicated by said command decoder front end, after receipt
10 of said command from said command decoder front end and
11 prior to said step of performing a second group of at least
12 one memory control step.

1 13. A method according to claim 8, further
2 comprising the step of said command decoder front end
3 selecting said first command sequencer from among a
4 plurality of parallel command sequencers in response to
5 receipt of said command packet.

6 14. A method for managing a memory system, for use
7 with a first incoming command packet, comprising the steps
8 of:

9 receiving said first incoming command packet in a
10 command decoder front end;

11 said command decoder front end decoding said first
12 command packet, issuing a command to a first command
13 sequencer in response to said first command packet, and
14 determining whether to perform a first group of at least

15 one memory control step in response to said first command
16 packet; and
17 said first command sequencer performing a second
18 group of at least one memory control step in response to
19 receipt of said command from said command decoder front
20 end.

1 15. A method according to claim 14, further
2 comprising the step of assembling said command packet from
3 a plurality of consecutive incoming command words.

1 16. A method according to claim 14, wherein said
2 command decoder front end determines to perform said first
3 group of memory control steps, further comprising the step
4 of said command decoder front end performing said first
5 group of memory control steps in response to said first
6 command packet,

7 wherein said second group of memory control steps
8 excludes said first group of memory control steps.

1 17. A method according to claim 16, wherein said
2 step of said command decoder front end issuing a command to
3 a first command sequencer in response to said first command
4 packet occurs substantially simultaneously with said step
5 of said command decoder front end performing said first

6 group of memory control steps in response to said first
7 command packet.

1 18. A method according to claim 14, wherein each of
2 said incoming command packets has associated therewith a
3 respective desired latency value, and wherein said command
4 decoder front end performs said step of determining whether
5 to perform said first group of memory control steps in
6 response to a determination of whether the desired latency
7 value associated with said first command packet is below a
8 predetermined threshold latency value.

1 19. A method according to claim 18, wherein said
2 command decoder front end determines that the desired
3 latency value associated with said first command packet is
4 below said predetermined threshold latency value, further
5 comprising the step of said command decoder front end
6 performing said first group of memory control steps in
7 response to said first command packet,

8 wherein said second group of memory control steps
9 excludes said first group of memory control steps.

1 20. A method according to claim 18, wherein said
2 command decoder front end determines that the desired
3 latency value associated with said first command packet is

not below said predetermined threshold latency value,
further comprising the step of said first command sequencer
performing said first group of memory control steps in
response to receipt of said command from said command
decoder front end.

21. A method according to claim 18, wherein said
incoming command packets include a command type indicator,
further comprising the step of wherein said command decoder
front end determining the desired latency value for said
first command packet in dependence upon the command type
indicator in the first command packet.

22. A method according to claim 14, further
comprising the steps of:

said command decoder front end further indicating a
latency value to said first command sequencer in
conjunction with said step of said command decoder issuing
a command to a first command sequencer; and

said first command sequencer inserting at least one
latency wait state in dependence upon said latency value
indicated by said command decoder front end, after receipt
of said command from said command decoder front end and
prior to said step of performing a second group of at least
one memory control step.

1 23. A method according to claim 14, further
2 comprising the step of said command decoder front end
3 selecting said first command sequencer from among a
4 plurality of parallel command sequencers in response to
5 receipt of said command packet.

1 24. A method of operating a memory device for use
2 in a packet-driven memory system comprising the steps of:
3 receiving external command packets in a command
4 front end circuit;

5 decoding said external command packets into internal
6 commands in said command front end circuit;

7 issuing said internal commands to respective
8 selected ones of a plurality of command sequencers;

9 receiving each of said internal commands from the
10 command front end circuit into the respective selected
11 sequencer;

12 performing a first group of control steps for a
13 respective given internal command decoded from each given
14 one of said external command packets, either in the command
15 front end circuit or in the sequencer selected for the
16 given internal command, selectably in dependence upon a
17 comparison of a latency value associated with the given
18 external command packet with a threshold latency value; and

19 performing a second group of control steps for the
20 given internal command in the sequencer selected for the
21 given internal command.

1 25. A method according to claim 24, further
2 comprising the steps of:

3 receiving in the command sequencer selected for each
4 given internal command a latency indication from the
5 command front end circuit; and

6 entering a wait state for a selected number of clock
7 cycles in dependence upon the command delay indication for
8 each given internal command, after receipt of the given
9 internal command in said step of receiving internal
10 commands, and prior to said step of performing a second
11 group of at least one memory control step.

1 26. A method for processing commands in a memory
2 system having a command module and multiple memory modules
3 coupled together via command and data links, the method
4 comprising the steps of:

5 issuing a command packet from the command module to
6 a selected memory module, the command packet having a
7 latency value associated therewith;

8 receiving the command packet in the selected memory
9 module via a command decoder front end;

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10         decoding the issued command packet into an internal
11     command;

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12 internally issuing the decoded command to a selected
13 one of a plurality of parallel functional units;

14 performing a first group of control actions in the
15 command decoder front end if the latency value is less than
16 a predetermined latency threshold; and

17 performing a remaining group of control actions in
18 the selected parallel functional unit.

1 27. A method of operating a memory device for use
2 in a packet-driven memory system comprising the steps of:

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3         receiving external command packets in a command
4 front end circuit;

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5      decoding one of the external command packets to
6      produce an internal command in the command front end
7      circuit;

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8 issuing the internal command to a selected one of a
9 plurality of command sequencers;

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10         performing a first group of control steps in the
11     command front end circuit;

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12 receiving the internal command from the command
13 front end circuit into the selected sequencer;

14 receiving a command delay output from the command
15 front end circuit into the selected sequencer;

16 entering a wait state for a selected number of clock
17 cycles if a latency value associated with the internal
18 command is greater than a predetermined latency threshold,
19 and
20 executing remaining control steps in the selected
21 command sequencer.

1 28. A method for generating a control signal
2 delayed by a delay time specified with a resolution smaller
3 than one period of a clock signal, comprising the steps of:
4 receiving a desired delay time specified as a
5 digital delay value which includes an m-bit integral
6 multiple and an n-bit fractional multiple of the period of
7 said clock signal, $m > 0$ and $n > 0$;
8 loading said m-bit integral multiple into a counter
9 clocked synchronously with said clock signal;
10 generating said control signal in response to count
11 completion of said counter; and
12 further delaying said control signal by $F/2^n \times T_{cp}$,
13 where F is the integer value of said n-bit fractional
14 multiple, and T_{cp} is the period of said clock signal.

1 29. A method according to claim 28, wherein said
2 step of further delaying said control signal comprises the
3 steps of:

4 providing said control signal to respective inputs
5 of N delay elements, each i'th one of said delay elements
6 inserting a respective relative delay of $((i-1)/N) T_{cp}$; and
7 selecting an output of the F'th one of said delay
8 elements.

1 30. A method according to claim 28, further
2 comprising the step of latching said n-bit fractional
3 multiple while said counter counts.

1 31. Selectable control signal delay apparatus, for
2 use with a delay value specified as a fixed point value
3 with m>0 integer bits carrying a value P and n>0 fraction
4 bits carrying a value F, comprising:

5 a counter having a load input port, a count output
6 port and a clock input, said load input port being coupled
7 to receive said integer bits and said clock input being
8 coupled to receive a clock signal having a clock period T_{cp} ;

9 a control signal generator coupled to generate said
10 control signal in response to count completion by said
11 counter; and

12 a fractional delay circuit coupled to receive said
13 control signal and said fraction bits, said fractional
14 delay circuit delaying said control signal by $F/2^n \times T_{cp}$.

1 32. Apparatus according to claim 31, wherein said
2 fractional delay circuit comprises N delay elements each
3 having an input coupled to receive said control signal,
4 each i'th one of said delay elements having an output and
5 inserting a respective relative delay of $((i-1)/N) T_{cp}$; and
6 a multiplexer coupled to receive the outputs of said
7 N delay elements, said multiplexer further having a select
8 input coupled to receive said fraction bits.

1 33. Apparatus according to claim 32, wherein the 1st
2 one of said delay elements consists of a conductor
3 connecting the input of said 1st delay element to the output
4 of said 1st delay element.

1 34. Apparatus according to claim 32, further
2 comprising a storage element having an input port coupled
3 to receive said fraction bits and an output port coupled to
4 the select input of said multiplexer.

1 35. Selectable control signal delay apparatus, for
2 use with a delay value specified as a 6-bit fixed point
3 value, comprising:

4 a counter having a load input port, a count output
5 port and a clock input, said load input port being coupled
6 to receive the high order 5 bits of said delay value and

7 said clock input being coupled to receive a clock signal
8 having a clock period;

9 a latch having a data input and a data output, the
10 data input of said latch being coupled to receive the low
11 order bit of said delay value;

12 a count completion detector coupled to generate a
13 control signal in response to count completion by said
14 counter;

15 a half-clock-period delay element having an input
16 and an output, the input of said half-clock-period delay
17 element being coupled to receive said control signal; and

18 a multiplexer having first and second inputs and a
19 select input, the first input of said multiplexer being
20 coupled to receive said control signal from said count
21 completion detector, the second input of said multiplexer
22 being coupled to the output of said half-clock-period delay
23 element.